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322454(22)

B. E. (Fourth Semester) Examination, April-May 2020

(New Scheme)

(CSE Branch)

COMPUTER SYSTEMS ARCHITECTURE

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Each question have four parts. Part (a) of each question is compulsory and carry 2 marks. Attempt any two parts from (b), (c) and (d) of each question.*

Unit-I

1. (a) What is computer system architecture? 2

(b) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400, a processor register R1 contain the number 200. Evaluate effective address if the addressing modes of the instruction are (i) direct; (ii) immediate; (iii) relative; (iv) register indirect. 7

(c) Analyze the various buses used in bus structure and express the importance of all buses. 7

(d) Write the differences between Hardwired and Micro programmed control unit. Draw the block diagram of both. 7

Unit-II

2. (a) Explain the array multiplication of positive binary operands in brief. 2

(b) Multiply 2 numbers (–9) and (–13) with the help of both algorithm. 7

(c) Explain IEEE floating point number representation and its operation for 32 bits. 7

(d) Evaluate the following by using Restoring Division : Divisor is 11 and Dividend is 1000 7

Unit-III

3. (a) Explain multimodule memory and interleaving. 2

(b) Explain the working of associative memory with block diagram and derive the expression for match logic. 7

(c) A two way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K X 32 :

(i) Formulate all pertinent information required to construct the cache memory.

(ii) What is the size of cache memory? 7

(d) Explain virtual memory in details. 7

Unit-IV

4. (a) Differentiate between synchronous and asynchronous data transfer. 2

(b) Define priority interrupt. Explain daisy chaining priority interrupt with a block diagram. 7

(c) What is direct memory access technique? Explain the rate of DMA controller with diagram. 7

(d) What is address space? Explain isolated v/s memory mapped I/O. 7

Unit-V

5. (a) Specify a pipeline configuration to carry out arithmetic operation $(A_i + B_i)\ (C_i + D_i)$. 2

(b) Consider the execution of the program of 15000 instructions a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline has 5 stages and that one instruction is issued per clock cycle. Calculate (i) speed up factor (ii) efficiency (iii) throughout. 7

(c) Draw and explain flow chart and timing diagram for the four segment instruction pipeline. 7

(d) Write short notes on 7

(i) Vector processor

(ii) Array processor